BRIEF DESCRIPTION OF THE DRAWINGS

These objects and other objects and advantages of the present invention will become more apparent upon reading of the following detailed description and the accompanying drawings in which:

FIG. 1 is a block diagram showing the structure of the main parts of an image encoder according to the first embodiment of the present invention;

FIG. 2 is a graph showing the relationship between the numbers of blocks and weighting coefficients, based on which the image encoder according to the first embodiment calculates weighting coefficients;

FIG. 3 is a graph showing the relationship between weighting coefficients and the distance between the center of a block and the center of a display screen, based on which the image encoder of the first embodiment calculates weighting coefficients;

FIG. 4 is a graph showing the relationship between quantization step widths and storage amounts in a transmission buffer, based on which the image encoder of the first embodiment calculates a function f(x);

FIG. 5 is a block diagram showing the structure of an image encoder according to the second embodiment of the present invention;

FIGS. 6A and 6B are diagrams each exemplarily showing an image input to a camera of a TV conference system or TV telephone system;

FIG. 7 is a diagram showing the structure of a circuit which employs a conventional image compression technique;

FIG. 8 is a diagram showing the structure of a circuit which employs another conventional image compression technique; and

FIG. 9 is a diagram exemplarily showing examples of quantization step width functions which are set by a function selector included in the circuit of FIG. 8.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will now be described with

reference to the accompanying drawings.

FIG. 1 is a diagram showing the structure of the main parts of an image encoder according to the first embodiment of the present invention.

As shown in FIG. 1, an image encoder 10 according to this embodiment comprises a frame divide circuit 11, a frame memory 12, a motion prediction circuit 13, an interframe prediction circuit 14, an orthogonal transformation circuit 15, a quantization circuit 16, an encoding circuit 17, a transmission buffer circuit 18, a buffer-storage amount detection circuit 19, a motion-vector-value memory 21, a motion-vector-based block grouping section 22 which groups blocks based on motion vector, a DC component memory 25, a DC-component-based block grouping section 26 which groups blocks based on DC component, a weighting coefficient calculation circuit 27 and a quantization step width calculation circuit 28.

The frame divide circuit 11, the frame memory 12, the motion prediction circuit 13, the interframe prediction circuit 14, the orthogonal transformation circuit 15, the quantization circuit 16, the encoding circuit 17 and the transmission buffer circuit 18 are connected in series, sequentially process image data input to the image encoder 10 so as to encode the input image data, and send the encoded image data from the transmission buffer circuit 18 to a transmission path.

The motion-vector-value memory 21, the motion-vector-based block grouping section 22, the DC component memory 25, the DC-component-based block grouping section 26, the weighting coefficient calculation circuit 27 and the quantization step width calculation circuit 28 constitute a weighting section 20 which is one of the features of the present invention. The weighting section 20 arranges blocks of the input image data into groups of blocks, which have the common properties to each other within the same group, based on the motion vector value detected by the motion prediction circuit 13 and the DC component calculated by the orthogonal transformation circuit 15, and calculates the weighting coefficient of each block. The calculated weighting coefficient is a

coefficient representing the importance of each block. The weighting section 20 determines the importance of each block, based on the motion vector value or the DC component, and assigns a large weighting coefficient to the block, determined to be highly important. Further, the weighting section 20 calculates the quantization step width necessary when the quantization circuit 16 quantizes the image data, based on the calculated weighting coefficient and data amount of the transmission buffer circuit 18 which is detected by the buffer-storage amount detection circuit 19. After this, the weighting section 20 provides the quantization circuit 16 with the calculated quantization step width.

Each circuit or section included in the image encoder 10 will now be described.

The frame divide circuit 11 divides one frame of the image data input to the image encoder 10 into an (N×M) number of blocks each having an (n×n) number of pixels. The frame divide circuit 11 writes each of the blocks into the frame memory 12, and inputs them to the motion prediction circuit 13.

The frame memory 12 sets the written blocks to be delayed by a single frame timing, and inputs the delayed blocks to the motion prediction circuit 13.

The motion prediction circuit 13 compares a block (target block) of a frame input from the frame divide circuit 11 with a block of a previously-input frame which is in the same position as the position of the target block and also with neighboring blocks of the previously-input frame, and finds out a block having the smallest difference from the target block, for each block included in the single frame input from the frame divide circuit 11. The motion prediction circuit 13 then calculates a movement direction and amount of the found block with respect to the target block and sets a motion vector between the two blocks, and writes a value of the motion vector into the motion-vector-value memory 21.

The interframe prediction circuit 14 detects the position of the found block in the previously-input frame based on the motion vector obtained by the motion prediction